REMARKS

This response is intended as a full and complete response to the non-final Office Action mailed April 12, 2005. In the Office Action, the Examiner noted that claims 27-35 and 48-54 are pending and rejected under 35 U.S.C. §§101 and 103. By this response, the Applicants have amended claims 27 and 48, and added new claims 55 and 56. The amendments to the claims and the new claims are fully supported by the Specification. For example, the amendments to the claims as supported at least by page 10, lines 13-23, and by page 11, line 33 to page 12, line 28. The new claims are supported at least by page 10, lines 9-12. Thus, no new matter has been added and the Examiner is respectfully requested to enter the amendments and the new claims.

In view of the above amendments and the following discussion, the Applicants submit that the claims pending in the application are believed to be directed to statutory subject matter and non-obvious under the respective provisions of 35 U.S.C. §101 and §103. Thus, the Applicants believe that the application is in condition for allowance.

It is to be understood that the Applicants, by amending the claims, do not acquiesce to the Examiner's characterizations of the art of record or to the Applicants' subject matter recited in the pending claims. Further, the Applicants are not acquiescing to the Examiner's statements as to the applicability of the art of record to the pending claims by filing the instant responsive amendments.

REJECTION OF THE CLAIMS UNDER 35 U.S.C. §101

The Examiner has rejected claims 27-35 under 35 U.S.C. §101 stating that "the claimed invention is directed to non-statutory subject matter." The Applicants respectfully traverse the rejection.

In particular, the Examiner finds the claims to be non-statutory "because they recite software components for programming a PLD, representing functional descriptive material without a computer readable medium or computer implemented method, program per se are not tangibly embodied."

However, the Applicants respectfully submit that claim 27 is direct to statutory subject matter for computer-related inventions, as generally described in MPEP 2106.

More specifically, the claim is a statutory process claim which is directed to a "Computer-Related Process Limited to a Practical Application in the Technological Arts" as described in detail in MPEP 2106.IV.B.2(b)(ii). Specifically, this section of the MPEP discloses (emphasis added below):

> "There is always some form of physical transformation within a computer because a computer acts on signals and transforms them during its operation and changes the state of its components during the execution of a process. Even though such a physical transformation occurs within a computer, such activity is not determinative of whether the process is statutory because such transformation alone does not distinguish a statutory computer process from a nonstatutory computer process. What is determinative is not how the computer performs the process, but what the computer does to achieve a practical application. See *Arrhythmia*, 958 F.2d at 1057, 22 USPQ2d at 1036."

MPEP 2106.IV.B.2(b)(ii) further discloses (emphasis added below):

> "For such subject matter to be statutory, the claimed process must be limited to a practical application of the abstract idea or mathematical algorithm in the technological arts. See *Alappat*, 33 F.3d at 1543, 31 USPQ2d at 1556-57 (quoting *Diamond v. Diehr*, 450 U.S. at 192, 209 USPQ at 10). See also *Alappat* 33 F.3d at 1569, 31 USPQ2d at 1578-79 (Newman, J., concurring) ("unpatentability of the principle does not defeat patentability of its practical applications") (citing *O'Reilly v. Morse*, 56 U.S. (15 How.) at 114-19). A claim is limited to a practical application when the method, as claimed, produces a concrete, tangible and useful result; i.e., the method recites a step or act of producing something that is concrete, tangible and useful. See *AT&T*, 172 F.3d at 1358, 50 USPQ2d at 1452. Likewise, a machine claim is statutory when the machine, as claimed, produces a concrete, tangible and useful result (as in *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601) and/or when a specific machine is being claimed (as in *Alappat*, 33 F.3d at 1544, 31 USPQ2d at 1557 (in banc). For example, a computer process that simply calculates a mathematical algorithm that models noise is nonstatutory. However, a claimed process for digitally filtering noise employing the mathematical algorithm is statutory."

Thus, a computer-related process claim comprises statutory subject matter if it produces a concrete, tangible and useful result. MPEP 2106.IV.B.2(b)(ii) further discloses an example of a process claim which meets this criterion (emphasis added below):

> "- A method of making a word processor by storing an executable word processing application program in a general purpose digital computer's memory, and executing the stored program to impart word processing functionality to the general purpose digital computer by changing the state of the computer's arithmetic logic unit when program instructions of the word processing program are executed."

Thus, a statutory computer-related process claim can include a claim in which a program is stored on a computer-related device which causes the computer-related device to have a changed functionality.

Similarly to the above example recited in MPEP 2106.IV.B.2(b)(ii), the subject matter of claim 27 is directed to a statutory method by which a programmable logic device may be programmed to have a changed functionality. As disclosed in the Specification of the present application (emphasis added below):

> "Programmable logic devices (PLDs), such field programmable gate arrays (FPGAs) and the like, are well known. A programmable logic device comprises a complex logical element that may be programmed to effect combinational logic, sequential logic, or combined combination and sequential logic functions. Thus, a PLD allows for software modifications of sequential and/or combinational logic in a physical layer. In this manner, bug fixes, feature enhancements, and other improvements to systems incorporating PLDs may be provided via software update." (page 1, lines 12-22)

Thus, by programming the programmable logic device, a system having the programmable logic device can experience, for example, "bug fixes, feature enhancements, and other improvements". Such bug fixes, feature enhancements and other improvements can change the functionality of the system having the programmable logic device. Thus, the method of claim 27 has a concrete, tangible and useful effect on the system having the programmable logic device.

Therefore, at least for the reasons discussed above, claim 27 comprises statutory subject matter. Moreover, claims 28-35 depend directly or indirectly from independent claim 27 and recite additional features thereof. As such, and at least for the same reasons set forth above with respect to the Applicants' independent claim 27, the Applicants submit that these claims also comprise statutory subject matter.

REJECTION OF CLAIMS UNDER 35 U.S.C. §103(a)

Claims 27-29, 31-35, 48-50, 53 and 54

The Examiner has rejected claims 27-29, 31-35, 48-50, 53 and 54 under 35 U.S.C. §103(a) as being unpatentable over Herrmann et al. (U.S. Patent No. 6,134,707, hereinafter "Herrmann") and further in view of Tang (U.S. Patent No. 6,389,321, hereinafter "Tang") and further in view of Sasaki (U.S. Patent 6,198,304, hereinafter "Sasaki"). The rejection is respectfully traversed.

The Applicants' independent claim 27 recites:

> "27. currently amended) A method for programming one or more programmable logic devices, comprising:
> programming a first file in a non-native format for programming said one or more programmable logic devices from a remote programmer source;
> converting said non-native format programmable logic instructions into a second file having programmable logic instructions in a format native to said programmable logic device;
> transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit;
> executing said converted file, for identifying particular target files associated with said programmable logic devices, via a first bus coupled to said switching circuits;
> enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus; and
> programming said identified programmable logic devices via a second bus coupled to said switching circuit."

The test under 35 U.S.C. §103 is not whether an improvement or a use set forth in a patent would have been obvious or non-obvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 110 USPQ 1021, 1024 (Fed. Cir. 1984) (emphasis added). Thus, it is impermissible to focus either on the "gist" or "core" of the invention, Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 USPQ 416, 420 (Fed. Cir. 1986) (emphasis added). Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties and the problem it solves. In re Wright, 6 USPQ 2d 1959, 1961 (Fed. Cir. 1988) (emphasis added). The combination of

Herrmann, Tang and Sasaki fails to teach or suggest the Applicants' invention as a whole.

Specifically, the Herrmann, Tang and Sasaki references, alone or in combination, fail to teach or suggest at least the "transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit" in combination with the "enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus" as recited in the claim as amended.

The Herrmann reference discloses an "apparatus and method for in-system programming of programmable devices" (Abstract). Specifically, the Herrmann reference discloses a "PCB 30 also includes an embedded controller 52 running interpreter software 54. The embedded controller 34 preferably includes JTAG interface circuitry (not shown). A bus 56 is used to route programming signals from the embedded controller 52 to the IC 50" (col. 4, lines 56-60). However, as the Examiner acknowledges, "Herrmann does not explicitly disclose ... executing the converted file for identifying particular target files associated with said programmable logic devices via a first bus coupled to switching circuits" (page 4 of the Office Action mailed on 4/12/2005). The Examiner also acknowledges that "[n]either Herrmann not Tang system discloses enabling switching circuits corresponding to said identifiers target files via said first bus" (page 5 of the Office Action mailed on 4/12/2005). The Applicants respectfully submit that the Herrmann reference also does not teach or suggest the use of both a first bus and a second bus coupled to the switching circuits of a plurality of functional elements each comprising a switching circuit coupled to a programmable logic device.

The Tang reference fails to bridge the substantial gap between the Herrmann reference and the present invention as recited in the claim. The Tang reference discloses that an "in-system programmable (ISP) system can be programmed by remote access from a host programming system" (Abstract). Specifically, the Tang reference discloses (emphasis added below):

> "While the control and programming data are received, the access interface provides the control and programming data as digital signals on

> a data bus (e.g., data bus 603) under the control of the microprocessor (e.g., microprocessor 605). The microprocessor, which executes a program stored in the non-volatile memory (e.g., EPROM 608), specifies an address on an address bus (e.g., address bus 604), so as to store the data on the data bus into memory (e.g., RAM 607). Step 2.2 is repeated until all control and programming data are stored into memory."

Thus, the Tang reference discloses an address bus and a data bus, but does not teach or suggest that both the address and data bus are coupled to each of a plurality of switching circuits which are each in turn coupled to a programmable logic device. As is evidenced by Figure 6 of the Tang reference, the address bus 604 and the data bus 603 are each directly (in the case of the data bus) or indirectly (in the case of the address bus) coupled to an ISP controller 402 which is in turn coupled to a plurality of programmable devices (i.e. ISP devices 404 and 405). Thus, the Tang reference does not teach or suggest the "transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit". The Tang reference does not teach or suggest a 1-1 correspondence between switching circuits and programmable devices. Therefore, the Tang reference also cannot teach or suggest the "enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus". Because the Tang reference does not teach a 1-1 correspondence between switching circuits and programmable logic devices, the Tang reference cannot teach or suggest enabling the switching circuit corresponding to each programmable logic device having the identified target files.

By contrast, the present invention teaches that each functional element comprises a programmable logic device coupled to a switching circuit and that the switching circuit corresponding to each programmable logic device having identified target files is enabled.

The Sasaki reference fails to bridge the substantial gap between the Herrmann and Tang references and the present invention as recited in the claim. The Examiner relies on the Sasaki reference to allegedly teach "in an analogous computer system enabling switching circuits corresponding to said identifiers target files via said first bus" (page 5 of the Office Action mailed on 4/12/2005). The Examiner in part cited Figures

6-9 to support the allegation. However, the applicants respectfully disagree. Nowhere in Figures 6-9 is there shown "transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit" in combination with the "enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus" wherein both a first bus and a second bus are coupled to the switching circuits of a plurality of functional elements each comprising a switching circuit coupled to a programmable logic device. Figures 6-9 show either (i) a single processor connected to a single PLD, but not coupled to both a data bus and an address bus, or (ii) multiple PLDs connected to a single processor/PROM.

Thus, the Herrmann, Tang and Sasaki references, alone or in combination, fail to teach or suggest the present invention, as claimed, as a whole.

Furthermore, the differences between the present invention and the cited references would not be obvious to one of ordinary skill in the art. The 1-1 correspondence between enabled switching circuits and programmable logic devices having the identified target files in part provides some of the advantages of the present invention. For example, as disclosed in the Specification of the present Application (emphasis added below):

> "Importantly, by utilizing the aforementioned JTAG physical layer and protocol to communicate between the processor board 122 and one or more PLDs 142 within the system 100, it is not necessary to include intelligence, such as a microprocessor, on the PLD host functional elements 140 within the system. In this manner, the decreased use of microprocessors within the system allows for a reduction in system cost." (page 13, line 29 to page 14, line 2)

In light of the reasons given above, independent claim 27 is nonobvious and allowable under 35 U.S.C. §103. Moreover, independent claim 48 containes substantially similar relevant limitations as those discussed above in regards to claim 27. Therefore, independent claim 48 is also nonobvious and allowable under 35 U.S.C. §103. Furthermore, claims 28-29, 31-35, 49-50, 53 and 54 under 35 depend directly or indirectly from independent claims 27 and 48 and recite additional features thereof. As

such, and at least for the same reasons set forth above with respect to the Applicants' independent claim 27, the Applicants submit that these claims are also non-obvious and allowable under 35 U.S.C. §103. Therefore, the Applicants respectfully request that the rejection be withdrawn.

Claim 52

The Examiner has rejected claim 52 under 35 U.S.C. §103(a) as being unpatentable over Herrmann, Tang, Sasaki and further in view of allegedly admitted prior art. The Applicants respectfully traverse the rejection.

Claim 52 is dependent directly upon independent claim 48. For at least the same reasons discussed above with respect to independent claim 48, dependent claim 52 is patentable under 35 U.S.C. §103(a) over Herrmann, Tang and Sasaki alone or in combination.

The Examiner alleges that "... admitted prior art discloses in an analogous computer system wherein said at least one programmable logic device is selected from the group consisting a gate array, field programmable gate array, programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices...." and that "[t]herefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selecting of devices is selected from the group comprising gate array as taught in admitted prior art in corresponding to programming PLD as taught in combination system by Herrmann, Tang, and Sasaki" (page 9 of the Office Action mailed on 4/12/2005).

However, the allegedly admitted prior art does also does not teach or suggest at least the transferring of the second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit, in combination with the enabling of the switching circuit corresponding to each programmable logic device having the identified target files via the first bus.

Therefore, the combined references fail to teach or suggest the Applicants' invention as a whole.

As such, the Applicants submit that dependent claim 52 is not obvious and is patentable under 35 U.S.C. §103 over the combination of Herrmann, Tang, Sasaki and further in view of allegedly admitted prior art. Therefore, the Applicants respectfully request that the rejection be withdrawn.

Claims 30 and 51

The Examiner has rejected claims 30 and 51 under 35 U.S.C. §103(a) as being unpatentable over Herrmann, Tang, Sasaki in view of technical paper published in May 1999, ver. 6, hereinafter called Altera Corporation. The Applicants respectfully traverse the rejection.

Claims 30 and 51 respectively depend directly from independent claims 27 and 48 and recite additional features thereof. As discussed above, the combination of Herrmann, Tang and Sasaki alone and in combination fail to teach or suggest the Applicants' invention as a whole.

The Altera reference fails to bridge the substantial gap between the Herrmann, Tang and Sasaki references and the Applicants' invention as recited in the independent claims. The Altera reference discloses that "[t]he Jam standard is a vendor- and platform-independent interpreted language optimized for programming devices via the IEEE std. 1149.1 (JTAG) interface. The Jam language allows a single Jam file (.jam) or Jam Byte-Code file (.jbc) to contain both the data to be programmed into a device and the algorithm required to accomplish programming." (see Altera, page 7, first paragraph).

However, the Altera reference also does not teach or suggest at least the transferring of the second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit, in combination with the enabling of the switching circuit corresponding to each programmable logic device having the identified target files via the first bus.

Therefore, the combined references fail to teach or suggest the Applicants' invention as a whole.

Therefore, the Applicants submit that claims 30 and 51 are not obvious and are patentable under 35 U.S.C. §103 over the combined references. Therefore, the Applicants respectfully request that the rejections be withdrawn.

NEW CLAIMS

New claims 55 and 56 are patentable at least because they depend directly from independent claim 27, which is patentable at least for the reasons given above.

CONCLUSION

In view of the foregoing amendments and remarks, the Applicants respectfully submit that the claims presently in this application are directed to statutory subject matter and are non-obvious under the respective provisions of 35 U.S.C. §§101 and 103. The Applicants believe that this application is in condition for allowance. Reconsideration of this application and its swift passage to issue are respectfully solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Eamon J. Wall or Stephen Guzzi at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

7/12/05

E J Wall

Eamon J. Wall
Attorney for Applicants
Reg. No. 39,414
(732) 530-9404

Moser, Patterson & Sheridan, LLP
Attorneys at Law
595 Shrewsbury Avenue
Suite 100
Shrewsbury, NJ 07702